PATENT ABSTRACTS OF JAPAN

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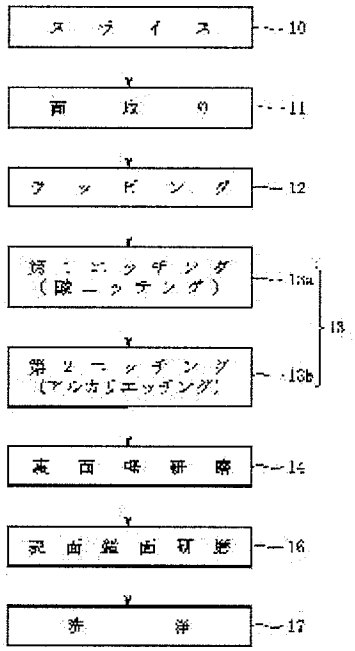
(54) METHOD FOR MANUFACTURING SILICON WAFER

(57)Abstract:
PROBLEM TO BE SOLVED: To give evenness with high accuracy and a small surface roughness on both surfaces of a wafer, and to visually distinguish the front and rear surfaces of a wafer.
SOLUTION: An improved method for manufacturing a wafer contains a slice step 10 of slicing a single-crystal ingot to obtain a thin disk-like wafer; a chamfering step 11 for chamfering the wafer; a lapping step of a levelling the wafer; an etching step 13 for removing a process distortion on a surface of the wafer; a surface-polishing step 16 for mirror-polishing one surface of the wafer; and a cleaning step 17 for cleaning the wafer. With this characteristic constitution, the etching step contains a first etching step 13a of acid-etching the wafer and a second etching step 13b for alkali-etching the wafer, after the first etching step. A backlight polishing step 14 for polishing a part of unevenness on the back of the wafer, formed by the etching step, is included between the etching step and the surface mirror-polishing step.



* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1]In a manufacturing method of a silicon wafer characterized by comprising the following, Said etching process (13) includes the 1st etching process (13a) that carries out acid etching of said wafer, and the 2nd etching process (13b) that carries out alkali etching of said wafer after this 1st etching process (13a), A manufacturing method of a silicon wafer including said etching process (13) and a rear-face light grinding process (14) of grinding a part of unevenness on a rear face of a wafer formed by said etching process (13) between said front surface mirror side polishing processes (16).
A slice step (10) which slices a monocrystal ingot and obtains a thin disc-like wafer.
A camfering process (11) of cutting off the corners a wafer obtained by said slice step (10).
A lapping process (12) which flattens said wafer cuted off the corners.
An etching process (13) which removes working distortion of a wafer surface introduced by said camfering process (11) and lapping process (12), and a surface polish process (16) of carrying out mirror polishing of said etched one side of a wafer and a washing process (17) which washes said wafer by which the surface polish was carried out.

[Claim 2]The manufacturing method according to claim 1 which sets polish cost on a rear face of a wafer by a rear-face light grinding process (14) to 1 micrometer or less.
[Claim 3]A sum total machining allowance of acid etching in the 1st etching process (13a) shall be 5-20 micrometers in the sum total with which the surface and a rear face of a silicon wafer were doubled, The manufacturing method according to claim 1 which sets a sum total machining allowance of alkali etching in the 2nd etching process (13b) to 5-25 micrometers in the sum total with which the surface and a rear face of a silicon wafer were doubled.
[Claim 4]Claims 1 thru/or 3 in which an etching reagent of acid etching in the 1st etching process (13a) contains fluoric acid and nitric acid, respectively are the manufacturing methods of a statement either.
[Claim 5]The manufacturing method according to claim 4 with which an etching reagent of acid etching in the 1st etching process (13a) contains further acetic acid, sulfuric acid, or at least one sort of phosphoric acid.
[Claim 6]Claims 1 thru/or 3 in which an etching reagent of alkali etching in the 2nd etching process (13b) contains sodium hydroxide or a potassium hydrate are the manufacturing methods of a statement either.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]There is this invention in providing the manufacturing method of the silicon wafer which has display flatness with highly precise wafer both sides, and small surface roughness, and makes the surface and rear surface of a wafer identifiable by viewing.
[0002]
[Description of the Prior Art]Generally the manufacturing process of a semiconductor silicon wafer, The wafer produced from the silicon single crystal ingot pulled up by starting and slicing is constituted from camfering, mechanical polishing (wrapping), etching, mirror polishing (polishing), and a process to wash, and it is produced as a wafer which has highly precise display flatness. Some of the processes are replaced by the purpose, or the multiple-times loop of these processes is carried out, or other processes, such as heat treatment and grinding, are added, they are replaced, and various processes are performed.
[0003]The silicon wafer which passed through machining processes, such as block cutting, outer diameter grinding, a slicing, and wrapping, has the damaged layer, i.e., a damaged layer, on the surface. Since a damaged layer induces crystal defects, such as slipping dislocation, in a device fabrication process, reduces the mechanical strength of a wafer and has an adverse effect on an electrical property, it must be removed thoroughly. An etching process is performed in order to remove this damaged layer. There are acid etching which uses acid etching liquid, such as mixed acid, and alkali etching using alkali etching liquid, such as NaOH, in an etching process. The etching rate depends for acid etching on the reacting species on the wafer surface in an etching solution, or the concentration gradient of a resultant greatly, and by the unevenness of the diffusion-zone thickness by causes, such as an uneven flow of an etching solution. An etching rate varies in a field, the display flatness obtained by wrapping is spoiled, and the unevenness called the wave of mm order and a peel to the etching surface occurs.
[0004]On the other hand, the etching rate does not depend for alkali etching on the reacting species of an etching solution, the concentration gradient of output, etc., but the display flatness of the wafer after etching is held with a high level. Therefore, in order to obtain high flatness, the alkali etching is superior to acid etching. However, in alkali etching, the pit (this is hereafter called facet.) whose sizes the local depth which appears depending on the crystal orientation of a wafer is a number - about 10 micrometers of numbers in several micrometers occurs. An etching rate is a dent which extremely unlike a facet originates in the ratio (crystal anisotropy) of the etching rate of <100>, <110>, and <111> becoming large, and is generated in crystal orientation <100>, crystal orientation <110>, and crystal orientation <111>. Not only a facet but the deep pit whose sizes are the depth and are 10 - about 10 micrometers of numbers in several micrometers or less is generated simultaneously. A deep pit is a deep hole which carries out the anomalous reaction only of the part, and produces it, when abnormal points, such as a local damage and a pollution source, remain on the surface of the silicon wafer.
[0005]Since the rear-face state formed of the etching process was maintained until it results in device fabrication, the following problems had generated it. Namely, if it sticks to an adhesive disk in the photo lithography process at the time of device fabrication, the wafer rear face by which acid etching was carried out, The wave of mm order formed in the wafer rear face of acid etching is transferred at the surface side, it appears as it is in the surface, and the wave of this mm order becomes the cause of reducing the resolution of exposure and reducing the yield of a device as a result. On the other hand, if

it sticks to an adhesive disk, a tip part with sharp unevenness of the facet on the big rear face of a wafer of surface roughness, a deep pit, etc. will be [the rear face] missing and carry out the raising dust of the wafer rear face by which alkali etching was carried out by chipping, much particle occurs and the problem that the yield of a device falls occurs. With the wafer after alkali etching, with the wafer by which mirror polishing was carried out, particle hardly generates both sides to the raising dust by about 4000-5000 particle and raising dust according to about 2000 particle with the wafer after acid etching occurring, and raising dust is not accepted.

[0006]Therefore, if mirror polishing of rear surface both sides of a wafer is carried out, since raising dust is suppressed since unevenness of big granularity does not exist in a wafer rear face, and the wave of mm order does not exist, either, high display flatness will be obtained and many problems by said etching will be solved, but. Since not only a wafer surface but a rear face will turn into a mirror plane if mirror polishing of rear surface both sides of a wafer is carried out, the problem that the wafer detecting sensor which detects existence of a wafer by dispersion of the light which has generally spread cannot detect a wafer occurs.

[0007]While making etching in an etching process into alkali etching as a method of solving such an above-mentioned problem, The manufacturing method of the semiconductor wafer incorporating the rear-face polishing process which removes a part of unevenness formed in the rear face of a wafer of alkali etching between the etching process and the surface polish process is proposed (patent number No. 2910507). It can become detectable [the wafer surface and rear surface by a wafer detecting sensor] by manufacturing a wafer using this method, while securing high display flatness, the raising dust by chipping on the back can be controlled, and the yield of a device can be raised.

[0008]

[Problem(s) to be Solved by the Invention]However, in the method shown in the patent number No. 2910507 gazette, since granularity became large when alkali etching was carried out, the machining allowance in the surface polish process had to be enlarged, and there was a problem to which the display flatness of polish DOWEHA which is a final product worsens. In order to consider it as predetermined rear-face granularity, there were a machining allowance of a rear-face polishing process and a problem which must be enlarged. As shown in drawing 4 (a), when etching the surface of the wafer in which abnormal points, such as a chip, a local damage, and a pollution source, remain in the end face etc., as shown in drawing 4 (b), crystal anisotropy serves as an etching surface which produced roundness centering on the part of a chip by small acid etching, but. As shown in drawing 4 (c), in alkali etching with large crystal anisotropy, the anomalous reaction was carried out from the part of a chip so that a deep pit might be formed, and there was a possibility of having produced a crack and a chip to some wafers and generating particle from the end face.

[0009]The purpose of this invention is to provide the manufacturing method of the silicon wafer which has display flatness with highly precise wafer both sides, and small surface roughness, and makes the surface and rear surface of a wafer identifiable by viewing.

[0010]

[Means for Solving the Problem]The slice step 10 which an invention concerning claim 1 slices a monocrystal ingot as shown in drawing 1, and obtains a thin disc-like wafer, The camfering process 11 of cutting off the corners a wafer obtained by the slice step 10, The lapping process 12 which flattens a wafer cuted off the corners, and the etching process 13 which removes working distortion of a wafer surface introduced by the camfering process 11 and the lapping process 12, It is improvement of a manufacturing method of a silicon wafer including the surface polish process 16 of carrying out mirror polishing of one side of an etched wafer, and the washing process 17 which washes a wafer by which the surface polish was carried out. This characteristic composition includes the 1st etching process 13a to which the etching process 13 carries out acid etching of the wafer, and the 2nd etching process 13b that carries out alkali etching of the wafer after this 1st etching process 13a, It is in a place including the rear-face light grinding process 14 of grinding a part of unevenness on a rear face of a wafer formed by the etching process 13 between the etching process 13 and the front surface mirror side polishing process 16.

[0011]In an invention concerning claim 1, an etching process is written with the 1st etching process by acid etching, and the 2nd etching process by alkali etching, Since wafer surface and rear surface granularity after etching becomes small, and generating of a deep pit can also be controlled and a machining allowance in a mirror-polishing process can be made small, high surface display flatness

obtained by wrapping is maintainable.
[0012]
[Embodiment of the Invention]Next, an embodiment of the invention is described based on a drawing. First, as shown in drawing 1, in order to cut a tip part and a trailer, to consider it as block like shape and to make the diameter of an ingot uniform, the raised silicon single crystal ingot grinds the outer diameter of an ingot, and uses it as a block body. In order to show specific crystal orientation, an orientation flat and an orientation notch are given to this block body. A block body is sliced with a predetermined angle after this process to the direction of a rod shaft (process 10). In order that the sliced wafer may prevent a chip and chip of the periphery of a wafer, chamfering work is carried out around a wafer (process 11). By performing this camfering, when growing epitaxially on the silicon wafer surface which is not cuted off the corners, for example, the crown phenomenon which abnormal growth happens to a periphery and rises to annular can be controlled. Mechanical polishing (wrapping) of the uneven layer of the wafer surface produced in the slice step 10 is carried out, and the display flatness of a wafer surface and the parallelism of a wafer are raised (process 12). The wafer which gave the lapping process 12 is washed and is sent to a next process.
[0013]Subsequently, chemical etching removes thoroughly the working distortion layer of the mechanical wafer surface introduced by the camfering process 11 and the lapping process 12 (process 13). The etching process 13 consists of the 1st etching process 13a that carries out acid etching of the wafer, and the 2nd etching process 13b that carries out alkali etching of the wafer after this 1st etching process 13a in the manufacturing method of this invention. Generating of a deep pit with few [and] facets with large shape on the surface of the wafer etched by the 1st and 2nd etching processes, respectively is also controlled. As for the etching reagent of the acid etching in the 1st etching process 13a, it is preferred that fluoric acid and nitric acid are included, respectively, and acetic acid, sulfuric acid, or at least one sort of phosphoric acid is included further. The etching reagent of the alkali etching in the 2nd etching process 13b contains sodium hydroxide or a potassium hydrate.
[0014]The sum total machining allowance of the acid etching in the 1st etching process 13a shall be 5-20 micrometers in the sum total with which the surface and the rear face of the silicon wafer were doubled, and the sum total machining allowance of the alkali etching in the 2nd etching process 13b shall be 5-25 micrometers in the sum total with which the surface and the rear face of the silicon wafer were doubled. It is preferred that the sum total machining allowance in the 1st etching process shall be 10-20 micrometers, and the sum total machining allowance in the 2nd etching process shall be 5-15 micrometers. Since the depth of the pit formed in the alkali etching (the 2nd etching) which follows that the sum total machining allowance in the 1st etching process is less than 5 micrometers does not become small, a polish machining allowance becomes large and the fault which is easy to worsen display flatness is produced, If 20 micrometers is exceeded, a wave (nano topography) will occur and fault will be produced at the time of device manufacturing (CMP process). The machining allowance of acid etching (the 1st etching) becomes it large that the sum total machining allowance in the 2nd etching process is less than 5 micrometers, the problem of a wave occurs, and if 25 micrometers is exceeded, the depth of a pit will produce the fault which becomes large. As for the wafer surface and rear surface which finished the etching process 13, unevenness is formed as shown in drawing 2 (a).
[0015]Next, the rear-face light grinding process of grinding a part of unevenness on the rear face of a wafer formed by the etching process 13 is performed (process 14). As shown in drawing 2 (b), granularity on the back is reduced by performing this rear-face light grinding to a wafer rear face. A single side grinding method is used in the front surface mirror side polishing process 16 following the rear-face light grinding process 14 of this invention, and the next. A single side grinding method is described based on drawing 3. This polish device 20 is provided with the rotary surface plate 21 and the wafer holding fixture 22. The rotary surface plate 21 is a big disk, and rotates by the shaft 23 connected focusing on the bottom. The abrasive cloth 24 is stuck on the upper surface of the rotary surface plate 21. The wafer holding fixture 22 consists of the shaft 22b which connects with the pressurizing head 22a at this, and rotates the pressurizing head 22a. The polishing plate 26 is attached to the undersurface of the pressurizing head 22a. The silicon wafer 27 of one sheet or two or more sheets adheres to the undersurface of the polishing plate 26. The piping 29 for supplying the grinding liquid 28 is formed in the upper part of the rotary surface plate 21. In grinding the silicon wafer 27 with this polish device 20, the pressurizing head 22a is descended, a predetermined pressure is applied to the silicon wafer 27, and it presses down the wafer 27. Supplying the grinding liquid 28 to the abrasive

cloth 24 from the piping 29, a uniform direction is made to rotate the pressurizing head 22a and the rotary surface plate 21, and the surface of the wafer 27 is ground evenly.
[0016]The polish cost on the rear face of a wafer by the rear-face light grinding process 14 shall be 1 micrometer or less. It is 0.3 micrometer or less preferably. If 1 micrometer is exceeded, a degree of brilliancy will not serve as a numerical value for which a device maker asks, but it will become difficult to attach distinction of a surface and rear surface. As this rear-face light grinding 14 shows the shape on the rear face of a wafer to drawing 3 (b), granularity on the back is stopped by the predetermined range.
[0017]The wafer which returned to drawing 1 and finished the rear-face light grinding process 14 is used as the mirror surface wafer which has optical gloss and does not have working distortion by carrying out mechanical mirror polishing which was, carried out and combined physical polish and chemical polish for the surface (process 16). The wafer which finished front surface mirror side polish is washed (process 17), and is sent to a device fabrication process.
[0018]
[Effect of the Invention]As stated above, in a wafer surface, a degree of brilliancy becomes high from a wafer rear face by passing through each processes 10-17 of this invention, Wafer both sides have highly precise display flatness and small surface roughness, and do not produce problems in detection of the wafer existence in the conveyance system of a device process, such as detection difficulty and wrong detection, but the surface and rear surface of a wafer can be differentiated to an identifiable grade by viewing.

[Translation done.]